DOCKET NO.: S1022.80888US01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	MARC PIAZZA AND PHILIPPE CORONEL	
Serial No.:	10/817,468	Patent No. 6,908,811
Filed:	April 2, 2004	Issue Date: June 21, 2005
For:	RAM	
Examiner:	David Nhu	
Art Unit:	2818	Confirmation No.: 3191

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: Pages 5 and 6 of 01/14/05 Amn and Col 14 of U.S. 6,908,811 B2
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617) 646-8000, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on the 27 day of June, 2005.

Gail Discoe

Attorney Docket No.: S1022.80888US01
XNDD

Respectfully submitted,

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REQUEST FOR CERTIFICATE OF CORRECTION

Sir/Madam:

Patentees respectfully request the correction of an error found in the above-captioned patent. Specifically, there is an error of omission in claim 15 of U.S. Patent No. 6,908,811 B2.

Column 14, claim 15, lines 47-55 are reproduced below:

> 15. A method as defined in claim 10, including, after depositing a conductive layer, the steps of:
> level trimming the structure to produce independent conductive surfaces between first and second neighboring trenches;
> depositing over an entire structure thus formed a thin dielectric with a high permittivity; and
> depositing over the entire structure a further conductive layer.

However, in the amendment filed January 14, 2005 claim 19 (claim 15 of the issued patent) reads as shown below.

> 15. A method as defined in claim 10, including, after depositing a conductive layer, the steps of:
> level trimming the structure to produce independent conductive surfaces between first and second neighboring **parallel** trenches;
> depositing over an entire structure thus formed a thin dielectric with a high permittivity; and
> depositing over the entire structure a further conductive layer. (Emphasis added)

No amendment was made by either the Examiner or Patentees deleting the word "parallel" from claim 15.

Support for the requested correction can be found in the enclosed, highlighted copy of: 1) pages 5 and 6 of the January 14, 2005 amendment and column 14 of issued U.S. Patent No. 6,908,811. Also enclosed is PTO form SB/44.

The correction requested does not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the correction be made and that a Certificate of Correction be issued.

Patentees respectfully submits that, since the error for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Certificate of Correction Branch, Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450 on the 17 day of June, 2005.

Respectfully submitted,

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Attorney Docket No.: S1022.80888US01
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layer, and an upper insulating layer;

forming, perpendicular to the parallel strips, in the upper insulating layer and at least a portion of the single-crystal semiconductor layer, first and second parallel trenches, each of the first and second parallel trenches being shared by neighboring cells;

forming, in each of the first parallel trenches, a first conductive line;

forming, in each of the second parallel trenches, a pair of second conductive lines, insulated from layers adjacent to the second trench;

filling the first and second parallel trenches with an insulating material;

removing remaining portions of the upper insulating layer; and

depositing a conductive layer.

15. (Currently amended) A method as defined in claim 14, wherein the first and second parallel trenches are formed so as to maintain a given thickness of the single-crystal semiconductor layer between the strongly conductive layer and ~~the~~a bottom of each of the first and second parallel trenches.

16. (Currently amended) A method as defined in claim 14, wherein the first and second parallel trenches are formed so as to partially expose the strongly conductive layer.

17. (Currently amended) A method as defined in claim ~~1~~14, including simultaneously forming the first conductive lines in each first trench and the pairs of second conductive lines in the second parallel trenches.

18. (Currently amended) A method as defined in claim 17, wherein simultaneously forming the first conductive lines and the pairs of second conductive lines includes:

depositing an insulating layer on ~~the~~a bottom and on ~~the~~ walls of the first and second parallel trenches;

conformally depositing a conductive material to at least fill the first trench; and

removing the conductive material from ~~the~~a surface of the first insulating layer.

19. (Currently amended) A method as defined in claim 14, including, after depositing

a conductive layer, the steps of:

level trimming the structure to produce independent conductive surfaces between first and second neighboring parallel trenches;

depositing over ~~the~~an entire structure thus formed a thin dielectric with a high permittivity; and

depositing over the entire structure a further conductive layer.

removing the first single-crystal semiconductor substrate, whereby the first insulating layer becomes an upper layer of the structure thus formed and the second insulating layer becomes a lower layer underlying the single-crystal semiconductor layer.

3. The method of claim 1, wherein the first and second parallel trenches are formed to maintain between the strongly-conductive layer and a bottom of each of the first and second parallel trenches a given thickness of the single-crystal semiconductor layer.

4. The method of claim 1, wherein the first and second parallel trenches are formed to partially expose the strongly-conductive layer.

5. The method of claim 1, including simultaneously forming the first conductive lines at a bottom of each first trench and the pairs of second parallel conductive lines at a bottom of the second parallel trenches.

6. The method of claim 5, wherein the simultaneous forming of the first conductive lines and of the pairs of second parallel conductive lines at the bottom of the first and second parallel trenches includes the steps of:

depositing at the bottom and on walls of the first and second parallel trenches an insulating layer;

conformally depositing a conductive material to at least fill the first trench; and

removing the conductive material from a surface of the first insulating layer.

7. The method of claim 5, wherein the first conductive lines formed at the bottom of the first parallel trenches are not insulated from layers peripheral to the first parallel trenches.

8. The method of claim 7, including the steps of:

conformally depositing an insulating material at the bottom and on walls of the first and second parallel trenches;

conformally depositing a first sub-layer of a conductive material;

performing a directional bombarding so that the conductive material is only bombarded on its sides in the second parallel trenches;

removing by selective etching non-bombarded portions of the conductive material in the first parallel trenches;

removing portions thus exposed of the insulating material previously deposited at the bottom of the first and second parallel trenches;

depositing a second sub-layer of the conductive material to at least fill the first parallel trenches; and

removing the conductive material from a surface of the first insulating layer.

9. The method of claim 1, including, after the step of deposition of a conductive layer, the steps of:

level trimming, which results in the forming, between first and second neighboring parallel trenches, of independent conductive surfaces in contact with a surface of the single-crystal semiconductor layer;

depositing over an entire structure thus formed a thin dielectric with a high permittivity; and

depositing over the entire structure a conductive layer.

10. A method for fabricating a monolithic DRAM-type memory, comprising:

forming, on a single crystal semiconductor substrate, parallel strips each including a lower insulating layer, a strongly conductive layer, a single crystal single-crystal semiconductor layer, and an upper insulating layer;

forming, perpendicular to the parallel strips, in the upper insulating layer and at least a portion of the single-crystal semiconductor layer, first and second parallel trenches, each of the first and second parallel trenches being shared by neighboring cells;

forming, in each of the first parallel trenches, a first conductive line;

forming, in each of the second parallel trenches, a pair of second conductive lines, insulated from layers adjacent to the second trench;

filling the first and second parallel trenches with an insulating material;

removing remaining portions of the upper insulating layer; and

depositing a conductive layer.

11. A method as defined in claim 10, wherein the first and second parallel trenches are formed so as to maintain a given thickness of the single-crystal semiconductor layer between the strongly conductive layer and a bottom of each of the first and second parallel trenches.

12. A method as defined in claim 10, wherein the first and second parallel trenches are formed so as to partially expose the strongly conductive layer.

13. A method as defined in claim 10, including simultaneously forming the first conductive lines in each first trench and the pairs of second conductive lines in the second parallel trenches.

14. A method as defined in claim 13, wherein simultaneously forming the first conductive lines and the pairs of second conductive lines includes:

depositing an insulating layer on a bottom and on walls of the first and second parallel trenches;

conformally depositing a conductive material to at least fill the first trench; and

removing the conductive material from a surface of the first insulating layer.

15. A method as defined in claim 10, including, after depositing a conductive layer, the steps of:

level trimming the structure to produce independent conductive surfaces between first and second neighboring trenches;

depositing over an entire structure thus formed a thin dielectric with a high permittivity; and

depositing over the entire structure a further conductive layer.

* * * * *

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Approved for use through 04/30/2007
U.S. Patent and Trademark Office; US. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,908,811 B2

DATED : June 21, 2005

INVENTOR(S) : Marc Piazza and Philippe Coronel

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 14, claim 15, line 50, should read:

--ductive surfaces between first and second neighboring parallel--

MAILING ADDRESS OF SENDER

PATENT NO. 6,908,811 B2

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